Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.046”**

**PAD FUNCTIONS:**

1. **A**
2. **B**
3. **C**
4. **N.G2A**
5. **N.G2B**
6. **G1**
7. **N. Y7**
8. **GND**
9. **N. Y6**
10. **N. Y5**
11. **N. Y4**
12. **N. Y3**
13. **N. Y2**
14. **N. Y1**
15. **N. Y0**
16. **VCC**

**14**

**13**

**12**

**11**

**2 1 16 15**

**7 8 9 10**

**3**

**4**

**5**

**6**

**MASK**

**REF**

**.058”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: FLOAT**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .046” X .058” DATE: 9/29/21**

**MFG: ZYTREX THICKNESS .025” P/N: 54HCT138**

**DG 10.1.2**

#### Rev B, 7/19/02